# 2023 SEE/MAPLD Workshop Call for Papers

## May 13 – 17, 2024

## San Diego Marriott La Jolla, La Jolla, CA

Please join us for 2024 Single Event Effects (SEE) Symposium and Military and Aerospace Programmable Logic Devices (MAPLD) Workshop to be held jointly May 13-17, 2024 in La Jolla, California.

We are seeking contributions in the areas below, but all submissions will be reviewed. Four sessions are available: ***SEE, MAPLD, Combined, and Poster.*** The Combined Session includes submissions that cross SEE and MAPLD themes. The Poster Session can include SEE, MAPLD, or Combined content. Please refrain from technical content reasonably classified as product marketing. Paper submissions are due on **February 23rd, 2024.**

We especially encourage submissions focusing on, but not limited to:

- Standards and methods (new or adapted)
- Heavy-ion, proton, and alternative SEE testing
- Test Facility Updates
- Space Environments
- Modeling and Simulation Approaches (new or adapted)
- Applications of AI/ML to SEE testing, analysis, and mitigation
- Mission Applications & Highlights Enabled by FPGAs/SoCs
- Device Failure Modes & Reliability
- Reconfigurable High-Performance Computing, Evolvable Hardware, & Security
- NextGen Platforms and Sensors Enabled by FPGAs/SoCs
- Tool Enablement

A Lightning Talks competition will be hosted this year, consisting of a three-minute presentation with a single slide. Submission details can be found on our website.

**Abstract Submission Guidelines:**

- Formats: Word (.docx), PowerPoint (.pptx), or (.pdf) only.
  - Word or PDF: 1-4 pages maximum.
  - PowerPoint: Title page with authors and affiliations, motivation/context/overview, available relevant results, and anticipated conclusions.
- Utilize templates available on our website.
- Submit online (https://www.seemapld.org/) before the deadline.

## Submission Deadline: Feb. 23rd, 2024

*The conference committee will attempt to notify all prospective speakers of acceptance status by March 31st.*

| SEE Symposium / Combined* / MAPLD Session Options | |
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| **Single-Event Phenomena, Mechanisms & Modeling:** Upsets, Functional Interrupts, Transients, Latchup, Gate Rupture, Burnout, etc. Destructive and Non-Destructive Effects, Nanoscale Phenomena, Charge Transport and Collection, Impact of Circuit and Environmental Parameters, etc. | **FPGAs/SoCs, PLDs, New Devices, and Design**: Novel FPGA and PLDs; Benchmarking; Applications of space-borne processing. Agile methods, ESL/HLS and model-based engineering techniques, embedded processing, and synthesis efficiency improvements. |
| **SEE Mitigation: Device Level** SEE Mitigation Methods including Radiation Hardened by Design (RHBD) and by Process (RHBP): Approaches for gaining SEE hardness in commercial devices, etc. | **SEE Mitigation: Circuit and System Level** Multi-level approaches for high reliability and fault tolerance (RHBD, redundancy, TMR, SET filtering, etc.), upset mitigation techniques, automated tools, etc. |
| **Environments and Facilities**: Space, Atmospheric, and Terrestrial environments. Heavy-Ion, Proton, Neutron, Pulsed Laser, and Other Test Facilities. Correlation between environment and test. | **Validation and Verification:** Techniques and languages such as co-simulation, System Verilog and OVM/UVM, etc. Simulation, emulation, new tools and methods for design validation. |
| **Device Data and Measurement:** Techniques for Memories, Analog/Digital Circuits, Systems-on-Chip (SoCs), FPGAs, Optocouplers, Photonic ICs, Power Converters, Sensors, etc. | **Availability, Reliability, and Susceptibility**: Failure mechanisms, reliability testing and characterization, packaging reliability, reliable design practices. |
| **Case Study: Devices and Systems:** Operational Regimes and Performance Data for Systems and Devices from LEO to Interplanetary, High Altitude Aircraft, and Terrestrial. | **Case Study: Computing, Logic, and Processing:** Novel applications of Reconfigurable computing, high-performance processing and successful deployment of programmable logic, etc. |
| **Systems and Error Rate Computation:** Error Mitigation, EDAC, Multi-core Processing, and Fault Tolerant Systems; Analytic, Monte Carlo, Mixed-Level, methods, etc. | **Research and Education:** Education Practices, Market Demands, and Retention. Training course overview and organization, Degree programs, Relevant future trainings 2024. |
| **Artificial Intelligence (AI) / Machine Learning (ML) in FPGAs/SoCs:** AI / ML design considerations for reliable terrestrial, avionic, and aerospace applications; using AI for SEE mitigation; SEE evaluation of designs leveraging AI / ML | |
| *All options subject to change any time, per the discretion of the conference committee | |

# 2024 Conference Committee

**Adrian Ildefonso**, NRL, SEE General Chair
**Paul Armijo**, Armijo Innovations LLC, MAPLD General Chair
**Krysten Pfau**, LMCO, SEE Technical Chair
**Tom Leahy,** SiFive**,** MAPLD Technical Chair
**Justin Likar,** JHU-APL, Tutorial Chair
**Martha O'Bryan**, SSAI/GSFC, Poster Session Chair
**Larissa Milic,** EMPC, Exhibit Chair
**Teresa Farris**, Archon, LLC, Meeting Planner
**Carl Szabo**, SSAI/GSFC, A/V Chair