Analysis of the Single Event Upsets in the Programmable Logic of 28-nm Xilinx Zynq-7000 FPGA due to Heavy Ion Irradiation

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Single Event Effects (SEE) Symposium &

Military and Aerospace Programmable Logic Devices (MAPLD) Workshop

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Motivation

- Increasing use of FPGAs in space avionics
  - FPGA vendors provide space-grade devices
    - e.g. Microsemi Flash RTG4 or Xilinx SRAM Virtex-5QV
    - extremely expensive and less efficient than the COTS SRAM FPGAs
  - State-of-the-art COTS SRAM FPGAs
    - e.g in CubeSat single-board computers
    - implement non-mission critical parts of the data processing modules

- Emerging trend of using Programmable SoC/MPSoC SRAM FPGAs
  - Xilinx APSoC Zynq-7000

- Radiation tests and SEE characterization are needed

Contributions

- Previous works (*) investigate SEEs in Zynq-7000 memories under heavy ion
- Our project goal is to analyze in-depth the SEEs in all the embedded memories of Zynq-7000
  - CRAM, BRAM, FFs (PL) and Caches, OCM (visible PS) and hidden PS memories (e.g. branch target buffer)
  - and evaluate the soft error vulnerability of an heterogeneous application (e.g. accelerator)
- Here, the SEU characterization of all the PL embedded memories with radiation testing
  - Calculate CRAM, BRAM, SRL, FFs cross section
  - Identify and separate upsets due to SETs (in global signals) from SEUs
  - Identify and analyze MBUs in CRAM

(*)

- Amrbar, Mehran, et al. "Heavy ion single event effects measurements of Xilinx Zynq-7000 FPGA." IEEE REDW, 2015.
- Tambara, Lucas Antunes, et al. "Heavy ions induced single event upsets testing of the 28 nm xilinx zynq-7000 all programmable soc." IEEE REDW, 2015.
- Stoddard, Aaron, et al. "A hybrid approach to FPGA configuration scrubbing." IEEE TNS, 2017.

Radiation test facility

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Beam features	CERN Super-Proton-Synchrotron North Area (SPS-NA)	GSI GSI Helmholtz Centre for Heavy Ion Research - Darmstadt
Date	16-18 Nov 2018	15 April 2019
Ion	Pb	Fe
Energy	150 GeV/c (1)	200 MeV/u
Flux (ions/cm²)	~10^3	~10^3
Size	~ 40 mm × 40 mm (2)	~32 mm × 32 mm
Beam period	~40 sec (3) (10 s on + 30 s off)	~3 sec (1 s on + 2 s off)

Comments

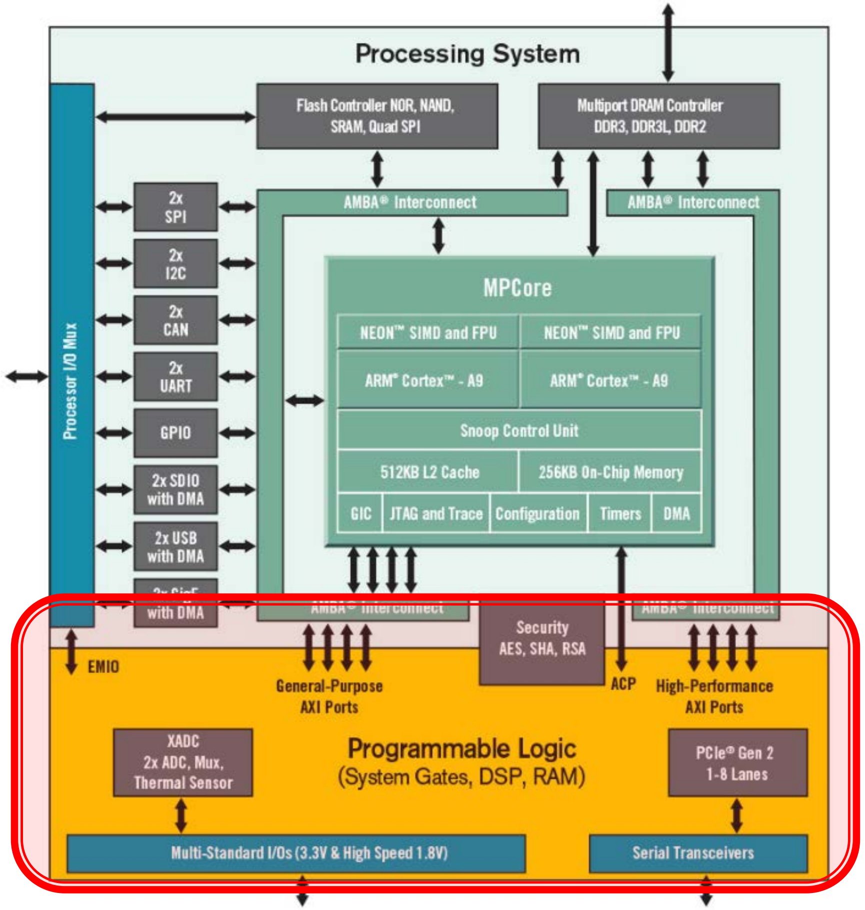
(1) High energy allows for testing in air, with packaged parts and tilting up to large angles

(2) No need for scanning (DUT size: < beam size)

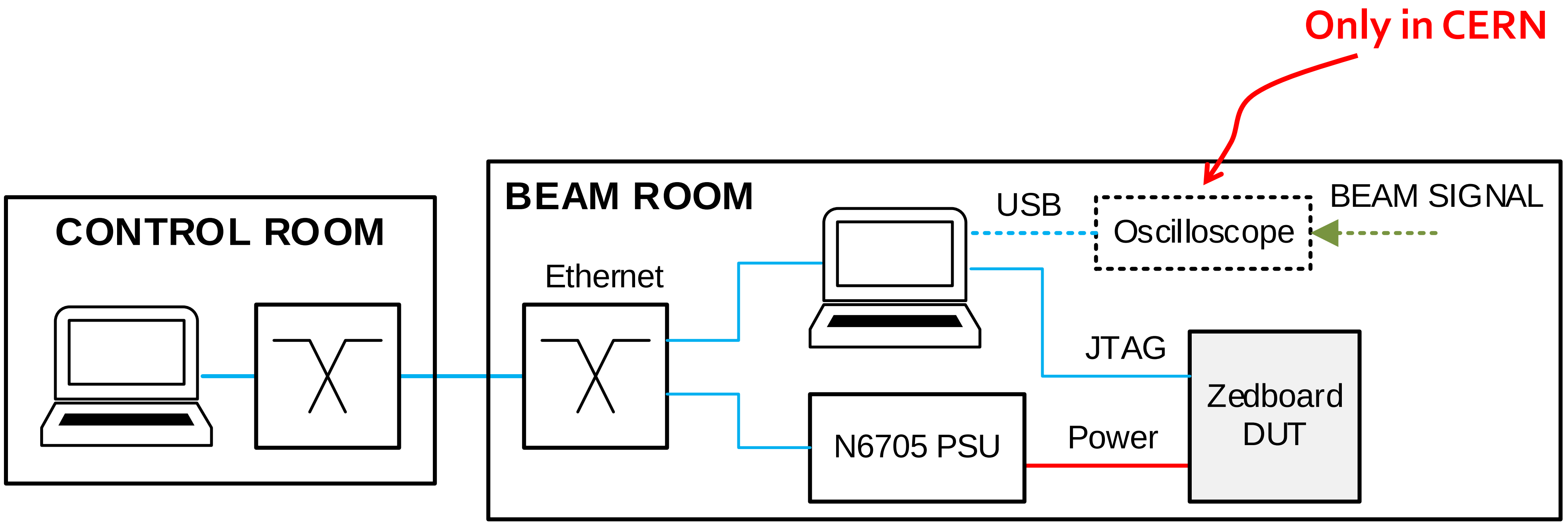
(3) CERN: Long enough idle period between spills to allow reconfiguration/scrubbing

Test setup - FPGA board

Radiation test	CERN	GSI
FPGA board	**Avnet Zedboard**	**Xilinx ZC706**
FPGA device	**XC7Z020**	**XC7Z045**
Package (size)	CLG484 (19x19 mm)	FFG900 (31x31 mm)
7-Series PL Equivalent	Artix-7	Kintex-7
Logic Cells	85K	350K
LUTs	53,200	218,600
Flip-Flops	106,400	437,200
BRAM	4.9Mb	19.2Mb
DSPs	220	900



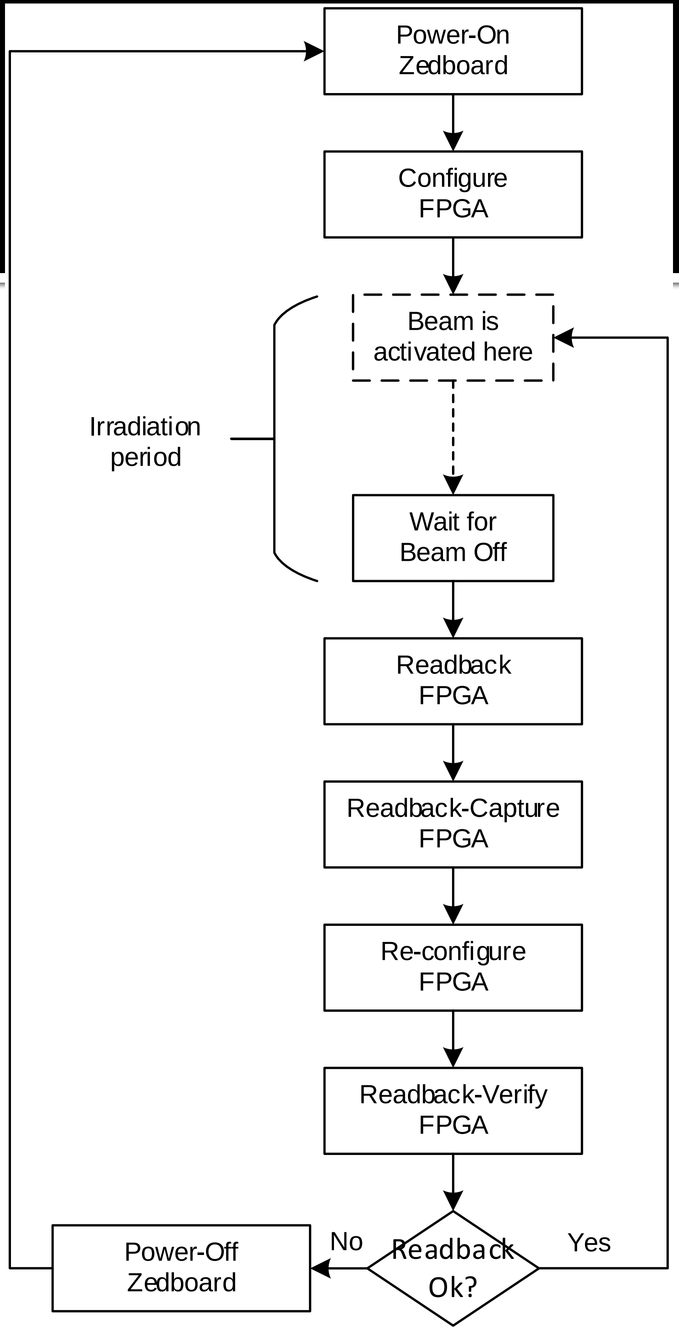
Test setup



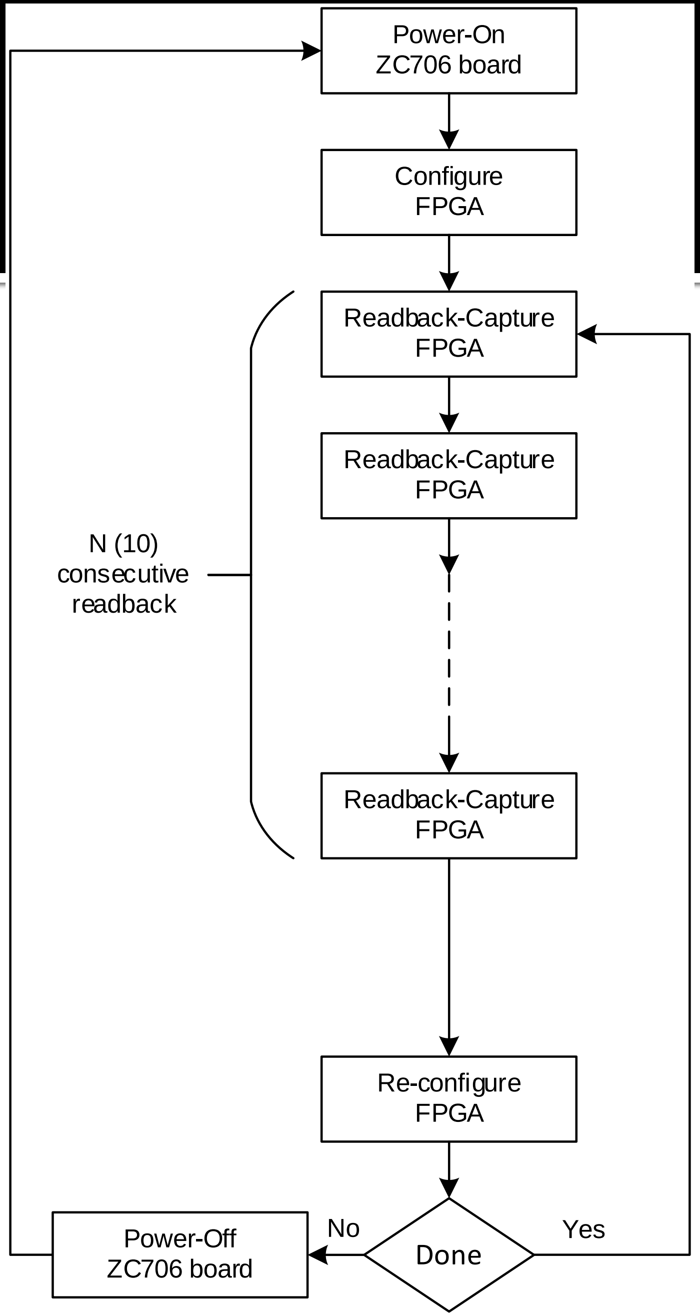
Only in CERN
CONTROL ROOM
BEAM ROOM
Ethernet
USB
Oscilloscope
BEAM SIGNAL
JTAG
Zedboard DUT
N6705 PSU
Power

Test flow

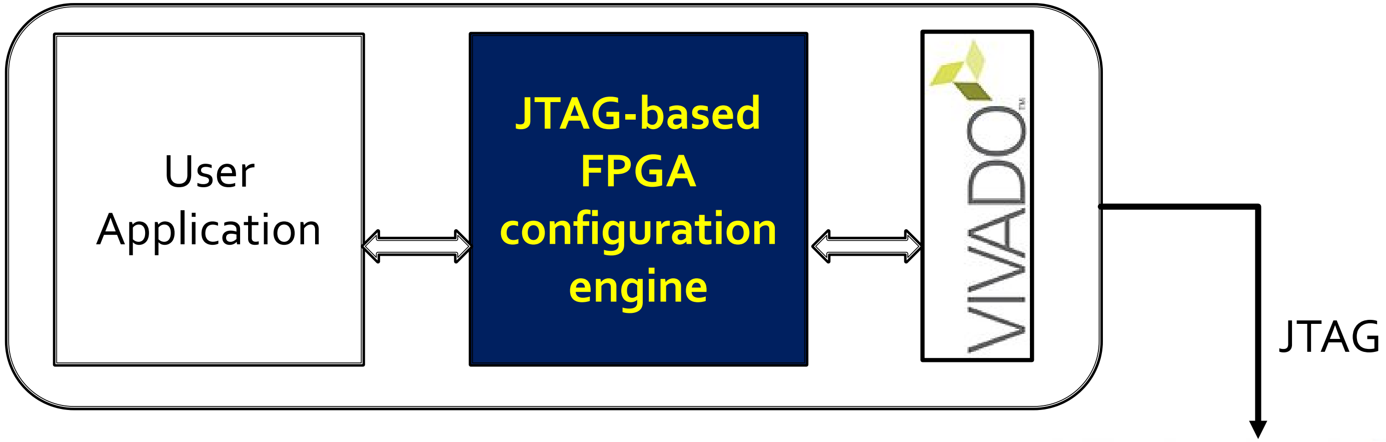
CERN:
Readback only during the beam off periods



GSI:
Continuous readback (every 10 readbacks reconfigure)



Test software (*)



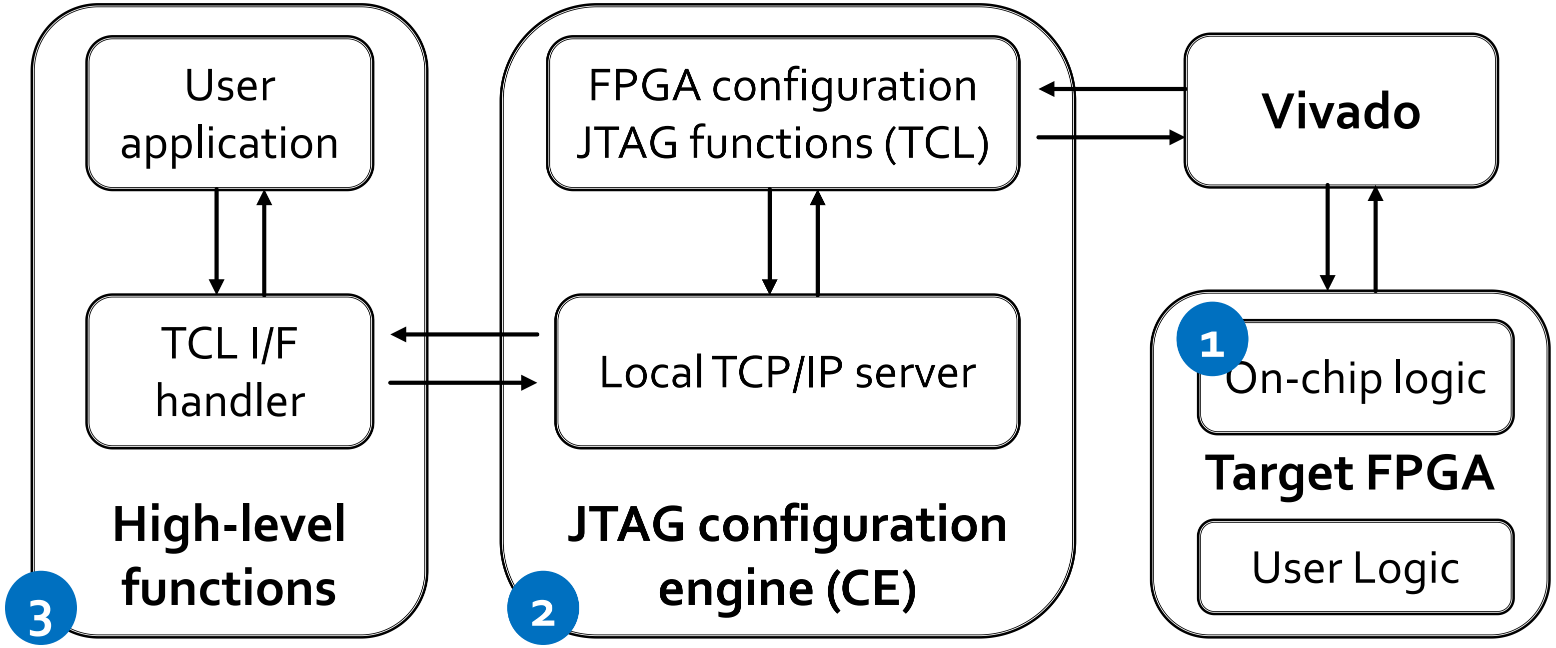
Developed a platform that provides access to the FPGA configuration memory through the JTAG:

- ✓ No extra equipment
- ✓ Minimum DUT modifications

(*) Open-source framework (GNU GPLv3 license):

FREtZ (FPGA Reliability Evaluation through JTAG) https://github.com/unipieslab/FREtZ

Test software

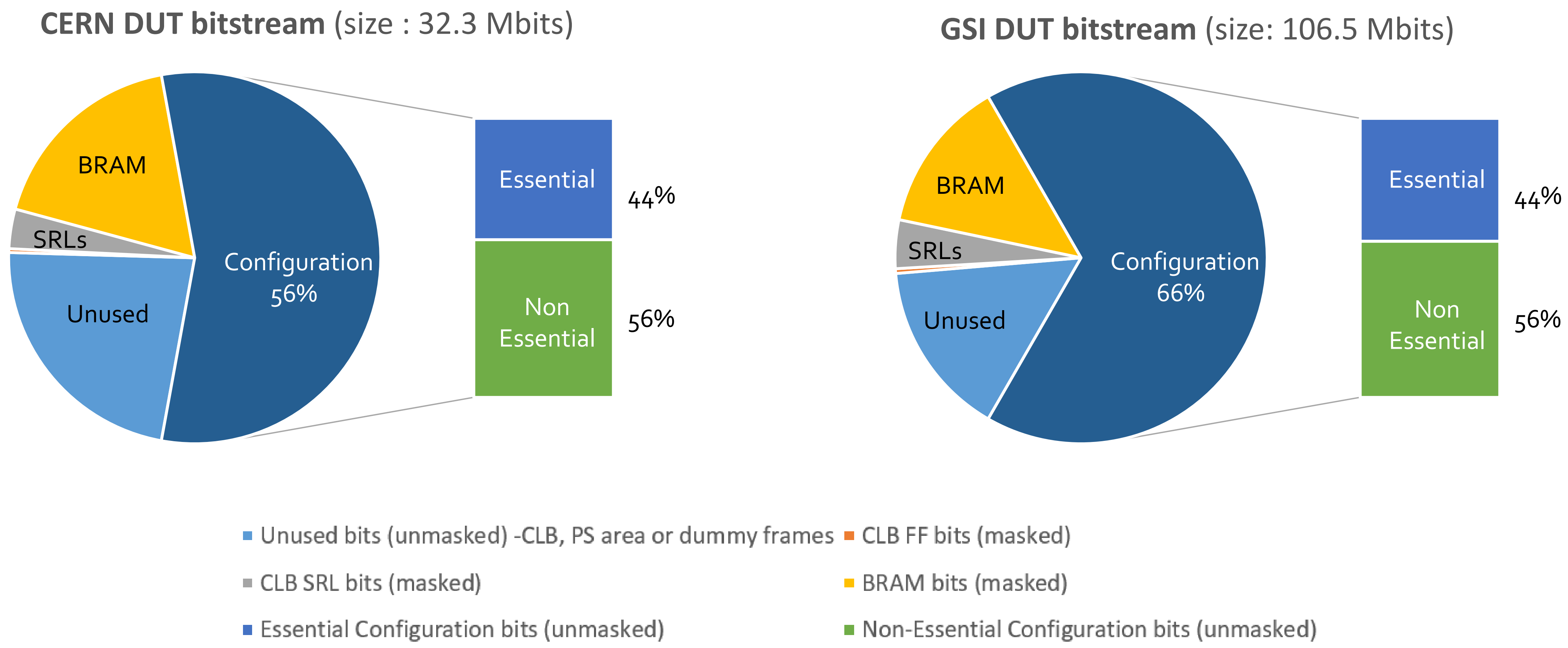


1. **On-chip logic**: access to the FPGA configuration memory through JTAG
2. **JTAG CE (server)**: low-level JTAG operations (TCL functions) through Vivado
3. **High-level app (client)**: user application and interface with JTAG CE

Benchmark

- High utilized and densely routed synthetic benchmark
  - 100% (slice, BRAM, DSP) utilization
- All slices are connected in long register chains
  - SLICEL LUTs as route-through -> CLB FFs -> SLICEM as 32-bit Shift Registers -> CLB FFs -> …
  - FFs-SRLs preloaded with specific patterns to calculate 0->1 and 1->0 likelihoods
    - continuous 0s or 1s or 0-1 patterns
  - To capture transients in the global signals (clock, reset)
    - CERN: CE of FFs/SRLs = 1, reset = synchronous
    - GSI: CE of FFs/SRLs = 1, reset/preset = asynchronous
- All BRAMs are instantiated and cascaded through the Data Bus
  - initialized to all 0s or 1s or checkerboard values
- All DSP slices are instantiated and cascaded
  - configured to implement MAC operation

Benchmark - bitstream



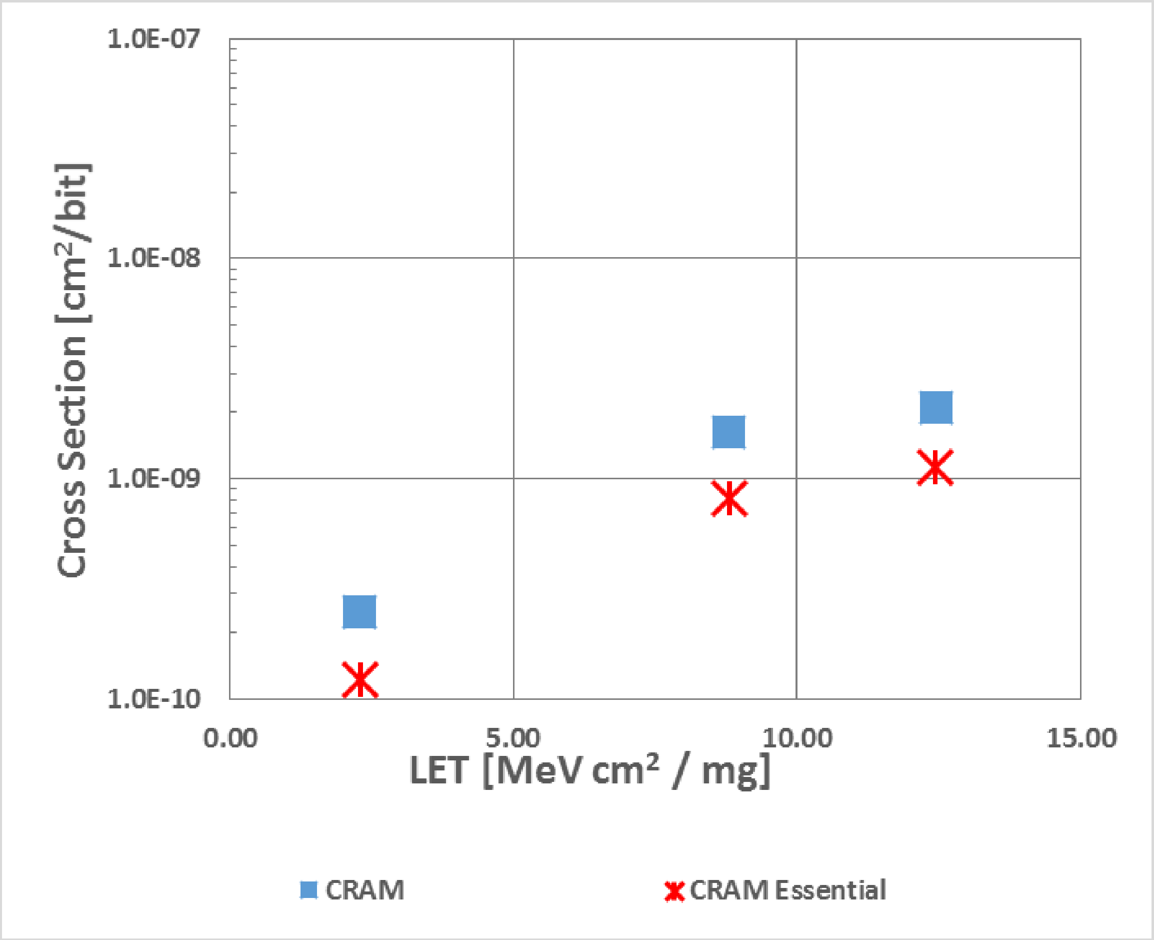
Test Sessions

Test	GSI	CERN	CERN
Angle of incidence (θ)	0^o	0^o	45^o
Runs	425	890	126
Total fluence (ions/cm²)	$\sim 3 \times 10^5$	$\sim 10^6$	$\sim 10^5$
Effective LET (MeVcm²/mg)	2.29	8.8	12.45

CRAM testing

CRAM upsets	GSI	CERN	CERN
LET	2.29	8.8	12.45
Fluence (ions/cm²)	~3x10⁵	10⁶	10⁵
Total	5953	27805	3351
Essential	2935	14057	1822

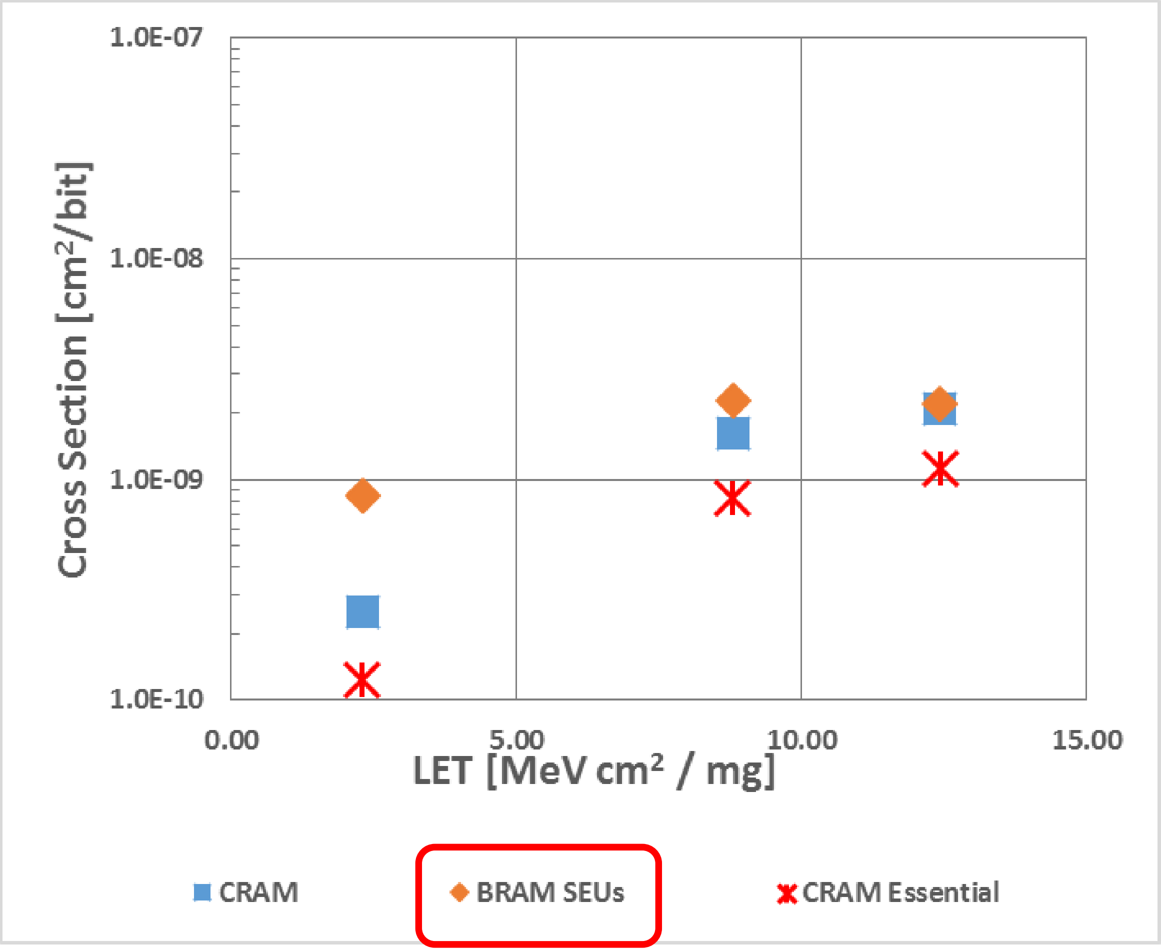
	Likelihood to upset 0->1 : 1 -> 0
CRAM	1 : 1.3



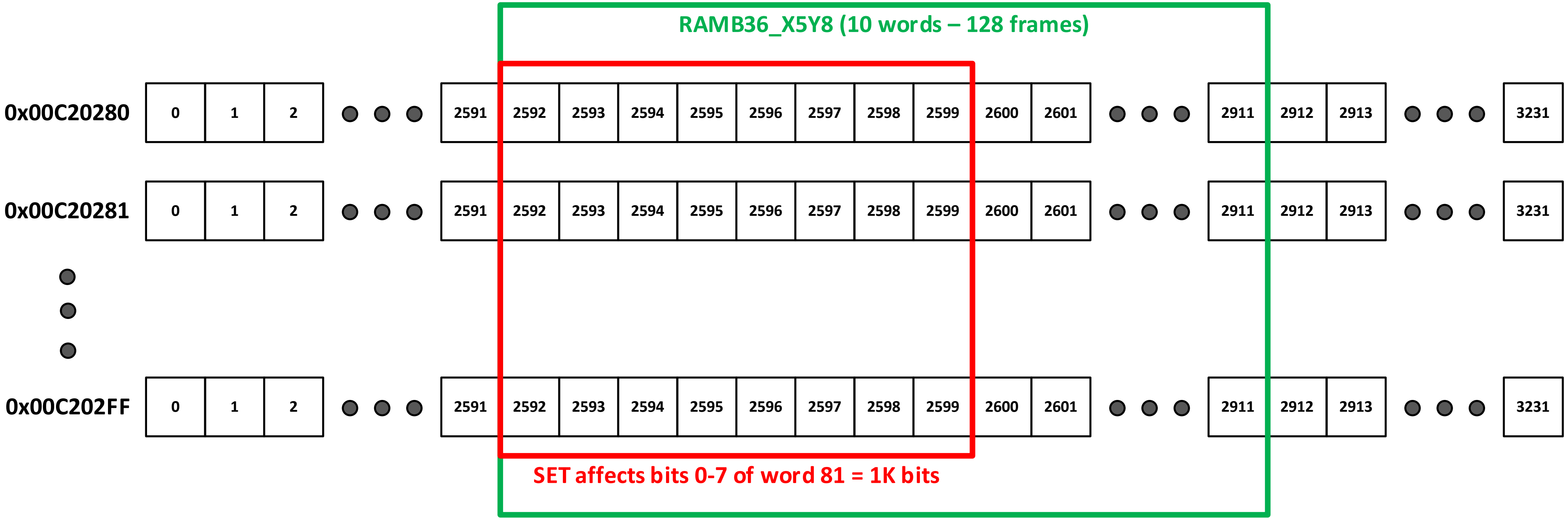
BRAM testing

BRAM upsets	GSI	CERN	CERN
LET	2.29	8.8	12.45
Fluence (ions/cm²)	~3x10^5	10^6	10^5
Upsets	4087	39142	7278
SEUs	4087	12509	1134

	Likelihood to upset 0->1 : 1 -> 0
BRAM	1 : 2.6



BRAM testing

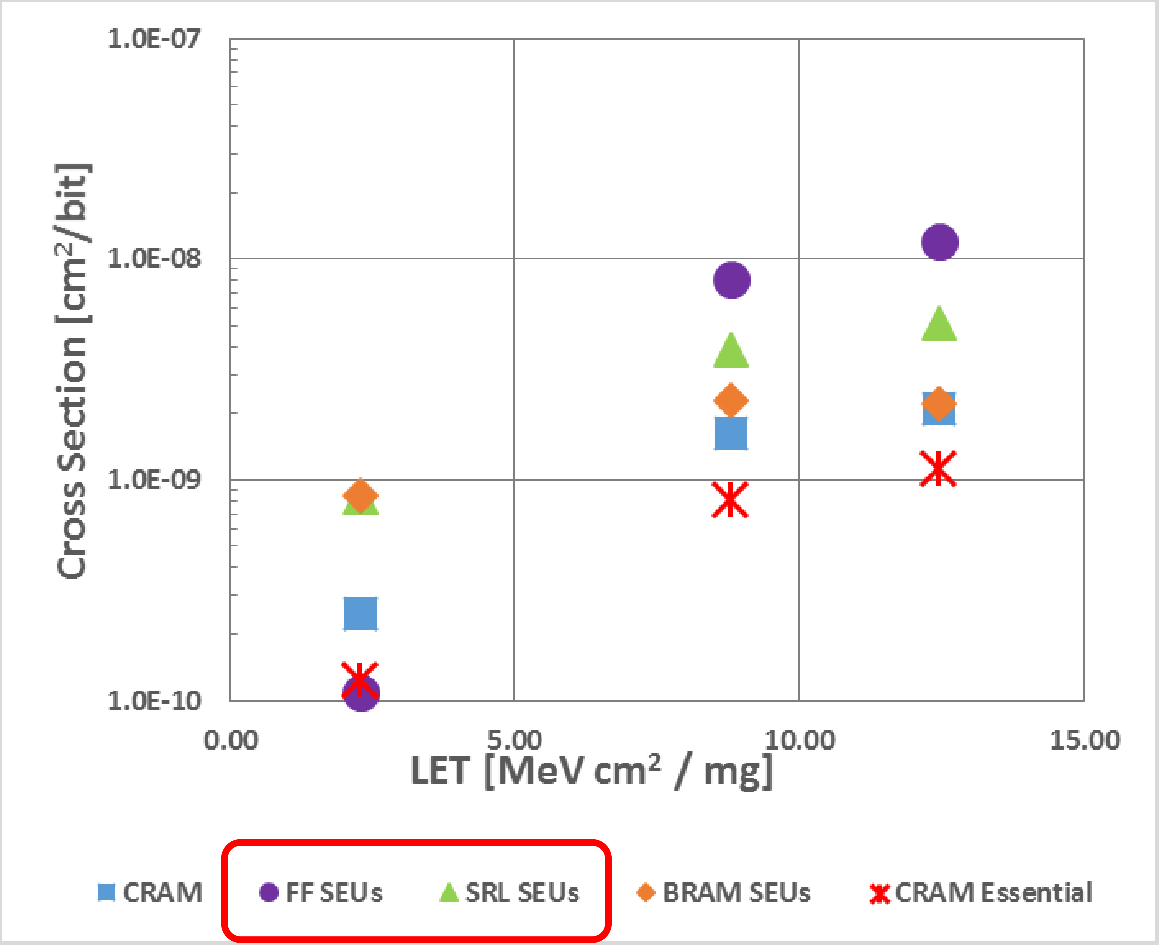


- Due to SET in clock signal
  - Upsets in 1K or 2K or 3K bits of the same BRAM
  - Always in 8 consecutive bits of 256 consecutive frames

FF & SRL testing

Upsets	GSI	CERN	CERN
LET	2.29	8.8	12.45
Fluence (ions/cm²)	~3x10^5	10^6	10^5
FF – Upsets	116	3743	258
FF - SEUs	16	818	114
SRL – Upsets	1268	16296	1094
SRL - SEUs	1268	4091	507

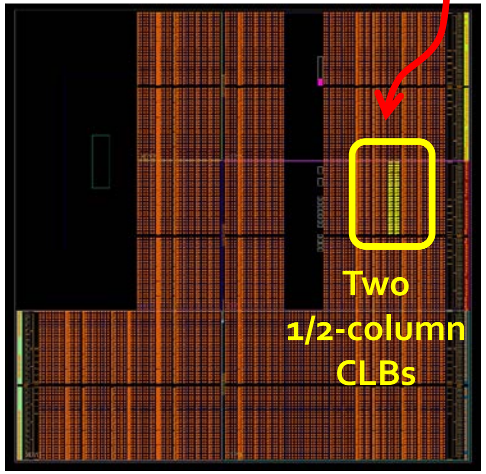
	Likelihood to upset 0->1 : 1 -> 0
FFs	1 : 1.9
SRLs	1 : 1

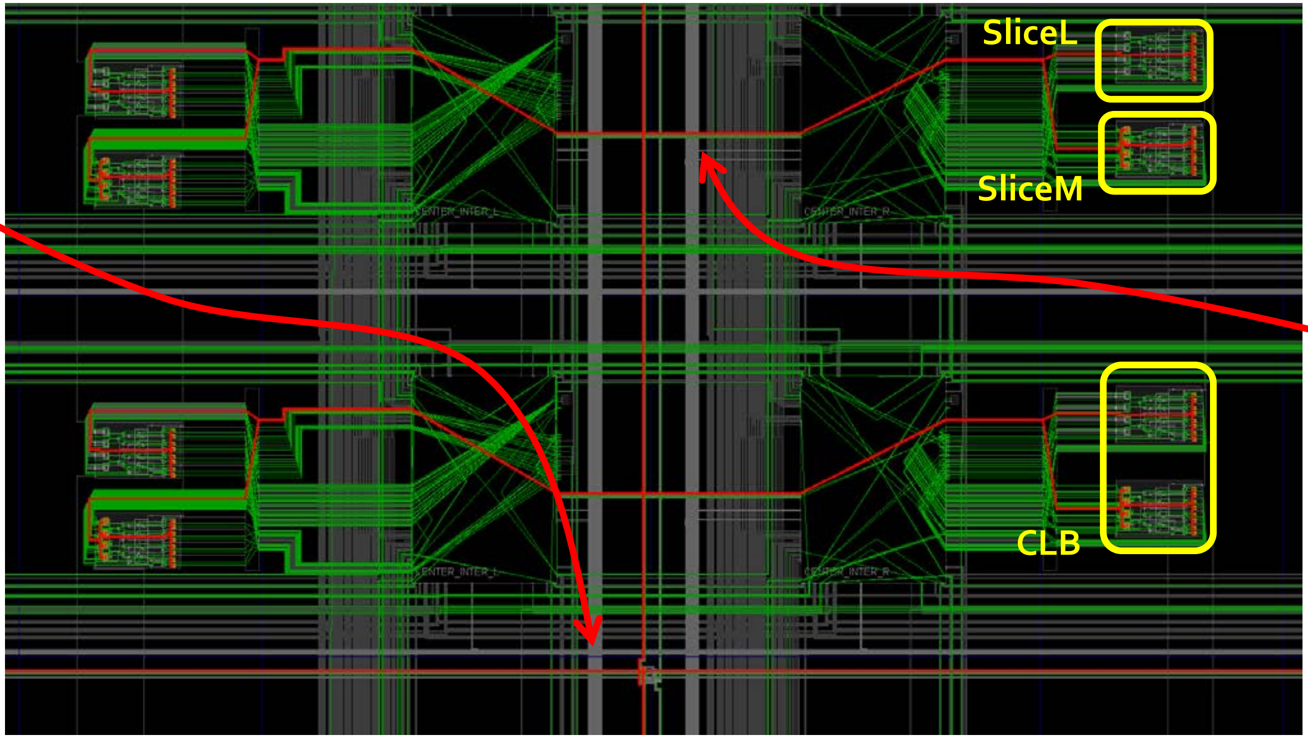


FF & SRL testing

SET in a CLB column clock net causes upsets in:

- One ½-column
  - 25x16=400FFs and/or
  - 3200 SRLs bits
- Two ½-column
  - 50x16=800FFs and/or
  - 6400 SRL bits





SET in a CLB clock net causes upsets in:

- 16 FFs and
- 4x32 SRL bits

MBU analysis

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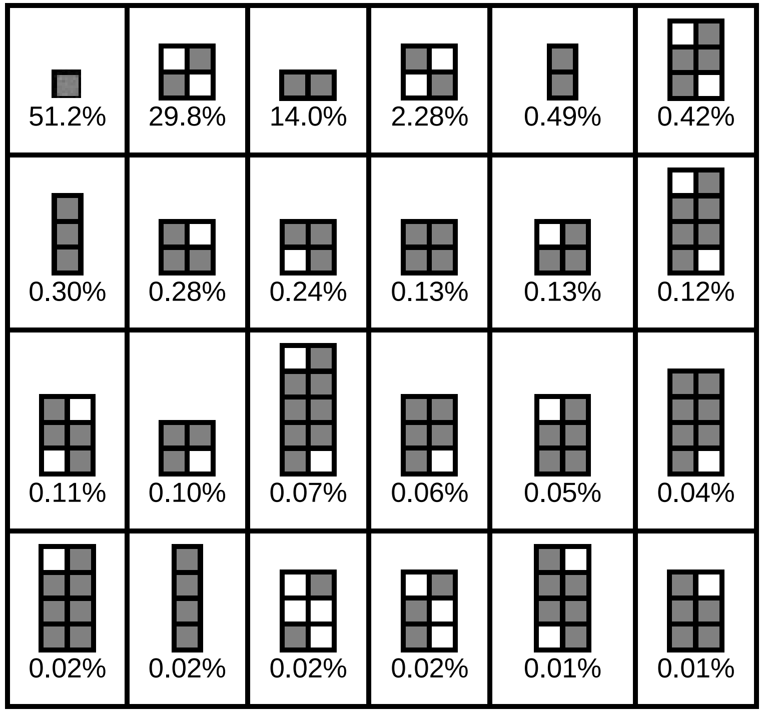
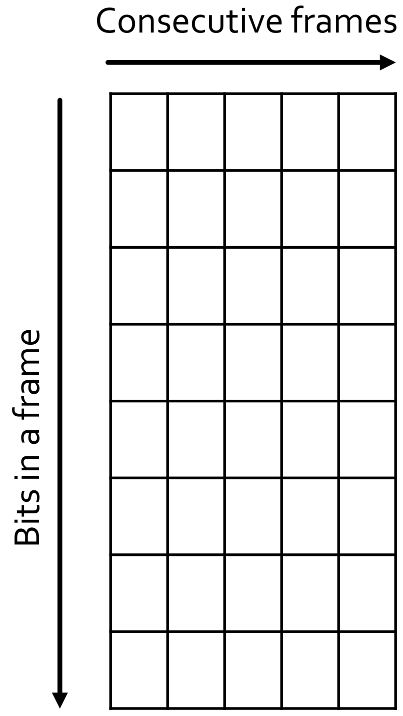
- Follow the method proposed here to identify MBUs (CERN results):
  - Wirthlin, Michael, et al. "A method and case study on identifying physically adjacent multiple-cell upsets using 28-nm, interleaved and SECDED-protected arrays." IEEE TNS, 2014

Upsets in a frame	# of Occurrences
1	28917
2	768
3	167
4	48
5	2

MBU shapes





Conclusions and future work

- Experiments provide a useful insight in the SEU sensitivity of the different embedded memories of the Zynq-7000
  - can be used to support the design of the fault tolerance architecture
    - MBU patterns can be used for the design of EDAC code or scrubbing approach
    - Upsets due SETs can be take into consideration from a TMR design
- More radiation experiments to be performed
  - With protons and for different LETs
- Embedded memories of the PS part will be also evaluated for SEUs

- Thanks for your attention!

QUESTIONS?