Tutorial Title:

Better FPGA Verification with Open Source VHDL Verification Methodology (OSVVM)

Abstract:

Verification consumes a considerable amount of the FPGA development cycle. Using an effective verification methodology is important as it can improve the overall productivity and contribute to the success of a project.

Open Source VHDL Verification Methodology (OSVVM) accelerates your FPGA and ASIC verification project by providing utility and model (Verification IP) libraries. Using these free, open source libraries you can create a simple, powerful, concise, and readable testbench that is suitable for either a simple FPGA block or a complex ASIC.

The OSVVM Utility Library uses a set of packages to create features that rival language based implementations (such as SystemVerilog and UVM) in both conciseness, simplicity, and capability. This presentation explores OSVVM's capabilities and why they are important:

- Transaction-Based Modeling
- Constrained Random test generation
- Functional Coverage with an API for UCIS coverage database integration
- Intelligent Coverage Random test generation
- Utilities for testbench process synchronization
- Utilities for clock and reset generation
- Transcript files
- Self-Checking – Alerts and Affirmations
- Message filtering – Logs
- Scoreboards and FIFOs (data structures for verification)
- Memory models

The OSVVM Verification IP Library is a growing set of transaction based models. Currently the repository has models and testbenches for

- AXI4 Lite: Master and Slave
- AXI Stream: Master and Slave
- UART: Transmitter and Receiver

Currently the OSVVM libraries are hosted on GitHub. With the IEEE 1076-2019 standardization effort, the 1076 packages are now IEEE Open Source. Following the path of IEEE 1076, OSVVM has been accepted as an IEEE Open Source project and will be migrating the primary Git repository to the IEEE hosted site sometime in Q1 2020.

Looking to improve your VHDL FPGA verification methodology? OSVVM provides a complete solution for VHDL ASIC or FPGA verification. There is no new language to learn. It is simple, powerful, and concise. Each piece can be used separately. Hence, you can learn and adopt pieces as you need them.

One question you may be asking yourself is, "How popular is VHDL and OSVVM for FPGA development?" The 2018 Wilson Research Group ASIC and FPGA Functional Verification Study [1] gave us the answer. World-wide, 62% of FPGA designs use VHDL, 45% of FPGA verification teams use VHDL, and 17% use OSVVM. For FPGA's clearly VHDL is popular and OSVVM is the #1 VHDL Verification Methodology.

[1] https://blogs.mentor.com/verificationhorizons/blog/2019/01/15/part-6-the-2018-wilson-research-group-functional-verification-study/

Author: Jim Lewis

Jim Lewis has 30 plus years of design and teaching experience and is well known within the VHDL community. He is the Chair of the IEEE 1076 VHDL Standards Working Group. He is a co-founder of the Open Source VHDL Verification Methodology (OSVVM) and the chief architect of the packages and methodology. He is an expert VHDL trainer for SynthWorks Design Inc. In his design practice, he has created designs for print servers, networking, fighter jets, video phones, and space craft.